UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/498,559	02/04/2000	Eduard Sackinger		8962

7590 06/03/2004

Docket Administrator (RM 3C-512)
Lucent Technologies Inc
600 Mountain Avenue P O Box 636
Murray Hill, NJ 07974-0636

EXAMINER	
LE, DINH THANH	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 06/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS
UNITED STATES PATENT AND TRADEMARK OFFICE
P.O. BOX 1450
ALEXANDRIA, VA 22313-1450
www.uspto.gov

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 20040523

Application Number: 09/498,559
Filing Date: February 04, 2000
Appellant(s): SACKINGER, EDUARD

EUGENE J. ROSENTHAL
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 27 February 2004.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The brief does not contain a statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief. Therefore, it is presumed that there are none. The Board, however, may exercise its discretion to require an explicit statement as to the existence of any related appeals and interferences.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

Appellant's brief includes a statement that claims 1-13 and 14-19 do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

6,069,516	Vargha	5-2000
6,028,496	Ko et al	2-2000

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 14-19 are rejected under 35 USC 102 (e) as being anticipated by Vargha (US 6,069,516).

Vargha discloses in Figure 1 a circuit comprising:

- a metal oxide semiconductor (MOS) transistor (12);

- a beyond voltage generator (10) which generates a beyond voltage (Vcc+V1) that is either greater than the highest voltage (Vcc) or less than the lowest voltage being supplied to said integrated circuit by a power supply; and

- wherein said MOS transistor (12) is coupled to said beyond voltage generator (10) so as to bias said MOS transistor with said beyond voltage (Vcc+V1) and said MOS transistor (10) is adapted to operate as said active inductor.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-13 are rejected under 35 USC 103 (a) as being unpatentable over Vargha (US 6,069,516) in view of Ko et al. (US Pat. 6,028,496).

Vargha discloses in Figures 1 and 2A-2B a circuit comprising:

- a metal oxide semiconductor (MOS) transistor (10) having a gate terminal, a drain terminal, and a source terminal, said drain terminal being coupled to a power supply voltage (Vcc);
- a beyond voltage generator (10) which generates a beyond voltage (Vcc+V1) that is greater than the supply voltage (Vcc); and
- wherein said circuit being adapted so that when said circuit is operating said circuit behaves as an active inductor between said source terminal and an other terminal of said active inductor on said integrated circuit.

However, Vargha does not disclose a resistor having a first terminal coupled to said gate terminal of the transistor (10) and a second terminal coupled to the beyond voltage (Vcc+ V1) that is derived from said power supply voltage (Vcc) as claimed. Ko et al teaches in Figure 2 an active inductor comprising resistors (R2, R4, R6, R8) coupled between the transistors (MT1-MT4) and a voltage divider (R1, R3, R5, R7, R9) for protecting the transistors from a rush currents from the voltage source (Vdd). It would have been obvious to a person having skill in the art at the time the invention was made to employ the resistor taught by Ko et al in the circuit of Vargha for the purpose of protecting the transistor.

(11) Response to Argument

a). The Appellant argues at pages 4-5 of the Appeal Brief that the circuit of Vargha operates as a switch not as an inductor because the transistor is not properly biased in a correct mode of operation such as the saturation mode. These arguments are not persuasive since

there is no limitation stated in the rejected claims that requires the MOS transistor to be biased in the saturation mode. Figure 1 of Vargha will perform the same function as the claimed circuit because both circuits have similar structures. Further, since the gate terminal of the MOS transistor (12) of Vagha is biased in the same condition as the gate terminal of the claimed transistor, i.e., by "a gate voltage (Vcc + V1) outside the range of a supply voltage (Vcc)", the circuit of Vargha would perform the function of an inductor when the transistor is turned on.

b). The Appellant argues at page 6, lines 13-29, that the function of the resistors (R2, R4, R6, R8) of Ko et al ascribed by the Office Action is not correct because the they are not used to protect the transistors from the rush currents and there is no motivation to combine the Ko et al reference with the Vargha reference. The arguments are not persuasive by the following reasons:

i. As shown on Figure 2, Ko et al suggests placing the resistors (R2, R4, R6, R8) between a voltage divider (R1-R9) and the transistors (MT1-MT4). Although Ko et al does not clearly disclose the function of the resistors (R2, R4, R6, R8), a person having skill in the art will readily recognize that the function of the resistors (R2, R4, R6, R8) is to reduce the rush currents or any surge currents introduced to the transistors when the supply voltage (Vdd) is switched on/off. Without the resistors (R2, R4, R6, R8) rush currents or surge currents can damage the transistors. Thus, the function of the resistors (R2, R4, R6, R8) is protection function. Moreover, the fact that Appellant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the

differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985).

ii. The Examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Vargha discloses a circuit comprising all of the limitations of the claimed invention as discussed above with the exception of the connection of a resistor between the gate terminal of the MOS transistor and the beyond voltage generator. While Ko et al suggests using this type of the resistors (R2, R4, R6, R8) in Figure 2 for the purpose of protecting the transistors from rush currents or surge currents. Thus, employing the resistor taught by Ko et al. in the circuit of Vargha to protect the MOS transistor would have been obvious to a person having skill in the art.

(12). Conclusion

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

DINH T. LE
PRIMARY EXAMINER

June 1, 2004

Conferred with SPE Callahan, Timothy

Chaudhuri, Olik OC